PROGRAMMABLE LOW-POWER HIGH-FREQUENCY DIVIDER

ABSTRACT

A fast latch including: a NAND stage adapted to receive a clock signal and a data input signal; a clocked inverter stage, a first input of the clocked inverter stage coupled to the output of the NAND stage and a second input of the clocked inverter stage coupled to the clock signal; a first inverter stage, a first input of the first inverter stage coupled to an output of the clocked inverter and a second input of the first inverter stage coupled to a reset signal; and a second inverter stage, having an output, an input of the second inverter stage coupled to an output of the first inverter stage. The fast latch is suitable for use in frequency divider circuits also described. A homologue of frequency dividers using the fast latch, a unique 3/4 divider and a 2 divider not using the fast latch are also disclosed.